Philadelphia University
Course Outline

Course Syllabus	
Course Title	Logic Circuits
Course Number	630211
Course Level	2nd year
Class Time	11:15 – 12:30 (M-W)
Instructor	Dr. Mohammed Bani Younis
email	mbaniyounis@philadelphia.edu.jo
website	www.philadelphia.edu.jo/academics/mbaniyounis
Prerequisites	Computer Skills I (710101)
Office Hours	Hours: 12:10-13:10 (Sun, Tue, Thu) and 09:45-11:15 (Mon-Wed) Office 725
Text Book	Digital Design, 4th Edition, M. Morris Mano and Michael D. Ciletti, Prentice Hall, 2007.

Course Goals:

The goal of the course is to Provide students with an introduction to the analysis and design of combinational and sequential digital logic circuits.

Time Schedule:

Duration: 16 weeks **Lectures:** 3 hours /week
Tutorial: None **Laboratories:**

Objectives:

At Completing this module the student should be able to :

1- Provide the student design methodologies for electronic circuits, to use mathematical expressions to describe the functions of simple combinational and sequential circuits.
2- Provide student with the approaches to converting numerical data from one format to another, to use different formats to represent numerical data.
3- Study Boolean algebra, basic laws and rules in logic design, DeMorgan's theorem, Karnaugh map, and approaches to simplifying logic circuits.
4- Study systematical design methodology for combinational logic circuits and build this kind of digital systems by using some IC devices.
5- Study systematical design methodology for sequential logic circuits.

Course Contents

		Week
❖	NUMBERS SYSTEMS AND CODES	1
❖	LOGIC SIGNALS ANS GATES	2
❖	COMBINATIONAL CIRCUIT ANALYSIS, (CIRCUIT MINIMIZATION, KARNAUGH MAPS.	2
❖	COMBINATIONAL LOGIC DESIGN PRACTICES, (DECODERS, ENCODERS, MUXS, AND DMUXS, ADDERS, SUBTRACTORS AND MULTIPLIERS).	3
❖	SEQUENTIAL LOGIC DESIGN PRINCIPLES: - LATCHES, SR FLIP-FLOP, JK FLIP-FLOP, AND D FLIP-FLOP - MASTER-SLAVE FLIP-FLOP, AND TRIGGERED FLIP-FLOPS	3
❖	SEQUENTIAL LOGIC DESIGN PRINCIPLES: (REGISTERS, SHIFT REGISTERS, AND COUNTERS)	3

Mode of Assessment

1-	**First Exam**	**20%**
2-	**Second Exam**	**20%**
3-	**Quizzes\Homework\ and or Projects**	**20%**
4-	**Final Exam**	**40%**

References

1- P. K. Lala, "Practical Digital Logic Design and Testing", Prentice Hall, 1996.
2- J. P. Hayes, "Introduction to Digital Logic Design", Addison-Wesley, 1996.
3- R. L. Tokheim, "Digital Electronics: Principles and Applications", 5th Edition, McGraw-Hill, 2000.